REMARKS/ARGUMENTS

Claims 1, 3, 5-9, 11, 13-20, and 22-25 are pending in the application. Claims 1, 11, and 20 are amended herein. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks/arguments.

In paragraph 5 of the final office action, the Examiner rejected claims 1, 3, 5, 7-9, 11, 14-20, and 22-25 under 35 U.S.C. § 103(a) as being unpatentable over Moeller (US2003/0170022, hereafter Moeller-022). In paragraph 6, the Examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Moeller-022 in view of Yonenaga. For the following reasons, the Applicant submits that all pending claims are allowable over the cited references.

Support for the amendment of claim 1 can be found, e.g., on page 5, lines 3-5; on page 10, lines 22-24; and in Figs. 4A-B. Claims 11 and 20 are amended similar to claim 1.

Claim 1 is directed to a method of signal processing. The method has the step of applying an **"AND" function** to the first and second bit estimate values to generate a bit of the bit sequence. Claim 1 also specifies that its processing applies to an optical signal having a **duty cycle greater than one**.

In the rejection of previously presented claim 1, on page 3 of the final office action, the Examiner admitted that Moeller-022 does **not** expressly disclose applying an **"AND" function** to the first and second bit estimate values to generate a bit of the bit sequence. However, on page 4, the Examiner stated that:

> Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) [and] the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability of a particular bit estimate value, e.g., "0" values.

In response, the Applicants submit that, as correctly noticed by the Examiner in the first of the above-cited passages, changing the application of an "OR" function to the application of an "AND" function requires a recognition of the fact that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors. However, that **recognition is absent** in Moeller-022 because Moeller-022 deals with decoding of optical return-to-zero (RZ) signals having a relatively small duty cycle, e.g., about 33% (see, e.g., Moeller-022's Figs. 3-4 and paragraphs [0018]-[0019]). When an optical signal has a small duty cycle, transmission impediments, such as jitter, do not increase the error probability for optical "zeros" (see, e.g., the last sentence of Moeller-022's paragraph [0026]). Therefore, there is no problem of incorrect decoding of optical "zeros" in Moeller-022, and it could not have been recognized there. In contrast, the present application recognized that, for optical signals having a duty cycle greater than one, incorrect decoding of optical "zeros" can be a major source of decoding errors (see, e.g., Applicants' Figs. 3A and 4A-B and page 5, lines 1-5).

However, on page 2 of the advisory action, the Examiner contends that "claim 9 of Moeller-022 discloses a scenario that employs non-return-to-zero (NRZ) pulses, which have a duty cycle of at least 100%."

The exact language from claim 9 in Moeller-022 is as follows: "The method of claim 8, wherein said input optical signal is a non-return-to-zero (NRZ) optical pulse." Thus, it is clear that claim 9 in Moeller-022 does not teach or even suggest the limitation of a duty cycle greater than one, the Examiner's assertion to the contrary notwithstanding. In fact, inspection of the entire specification in Moeller-022 shows that the term "**duty cycle**" is **not mentioned** there at all. The only examples in Moeller-022 from which the duty cycle can be inferred are shown in Figs. 1, 3, and 4. The example shown in Fig. 1 has a label "10 Gb/s 33% RZ TX," the most reasonable interpretation of which is that it refers to a return-to-zero signal having a duty cycle of 33%. The duty cycle for the examples shown in Figs. 3 and 4 can be estimated as a ratio of the pulse width to the bit-slot width. That ratio and therefore the duty cycle does not exceed 50% by any measure.

To summarize, Moeller-022 (i) does **not recognize** that incorrect decoding of optical zeros can be a major source of decoding errors, (ii) does **not** disclose that an **"AND" function** can be used to correct decoding errors, and (iii) does **not** teach or suggest that the error-correction method disclosed therein is applicable to optical signals having a duty cycle **greater than one**. The Applicants submit that, in the absence of these teaching and suggestions, it would not have been obvious to one of ordinary skill in the art to arrive at the invention of claim 1 from the disclosure of Moeller-022.

For all these reasons, the Applicants submit that claim 1 is allowable over Moeller-022. For similar reasons, the Applicants submit that claims 11 and 20 are also allowable over Moeller-022. Since the rest of the claims depend variously from claims 1, 11, and 20, it is further submitted that those claims are also allowable over Moeller-022. The Applicants submit therefore that the rejections of claims under § 103 have been overcome.

In view of the above remarks/arguments, the Applicants believe that the pending claims are in condition for allowance. Therefore, the Applicants believe that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

During the pendency of this application, the Commissioner for Patents is hereby authorized to charge payment of any filing fees for presentation of extra claims under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17 or credit any overpayment to **Mendelsohn & Associates, P.C. Deposit Account No. 50-0782**.

The Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR §§ 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Respectfully submitted,

Date: 10/05/2007
Customer No. 46850
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

/Yuri Gruzdkov/
Yuri Gruzdkov
Registration No. 50,762
Attorney for Applicant
(215) 557-8544 (phone)
(215) 557-8477 (fax)